() Preliminary Specifications
(V) Final Specifications

Module	**11.6”(11.57”) HD 16:9 Color TFT-LCD with LED Backlight design**
Model Name	A116XW02 V.0

Customer	**Date**
Checked & Approved by	**Date**
Note: This Specification is subject to change without notice.	

Approved by	**Date**
Debbie Chou	*2011/01/17*
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Contents

Record of Revision

Version and Date	Page	Old Description	New Description
0.0 2010/03/17	All	First Draft	All
0.1 2010/03/22	13	LED Power Supply: 12.6	LED Power Supply: 13.5
	17	Pin 27/28	Update description
	18	Clock frequency	Typ.: 70, max.: 80
0.2 2010/0702	5	White Luminance and Weight	Updated
	6	Viewing Angle	Values of upper and lower exchanged
	12	Drawing	Update a clearer one
	13	5.2.2 Backlight input signal characteristics	Updated
		Condition of LED life time	Updated
	14~15	VSYNC/HSYNC in the Table/Drawings	Deleted and Updated
	17	Pin 27/28	Updated
	17	Note	Added
	18	6.4.1 Timing Characteristics	Updated
	21~22	8. Mechanical Characteristics	Updated
	23~24	9. Shipping and Packing	Updated
0.3 2010/07/15	13	LED Life Time	Updated
0.4 2010/10/05	21	8. Mechanical Characteristics	Updated
1.0 2010/10/21	6	2.2 Optical Characteristics	Updated
1.1 2011/01/17	5	White Luminance	Updated

Record of Revision

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostic breakdown.

2. General Description

A116XW02 V0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1366(H) x768(V) screen and 262k/16.2M colors (RGB 6-bits/6-bits+FRC data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

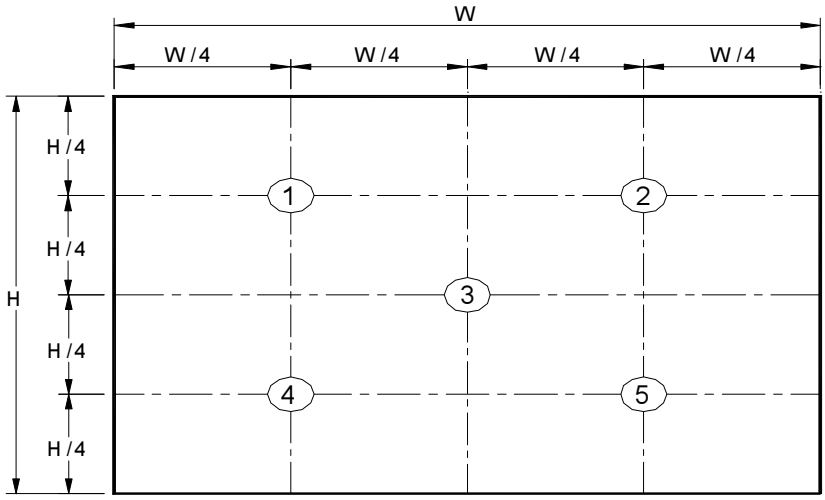
Items	Unit	Specifications
Screen Diagonal	[mm]	293.83
Active Area	[mm]	256.125 X 144.0
Pixels H x V		1366x3(RGB) X 768
Pixel Pitch	[mm]	0.1875 X 0.1875
Pixel Format		R.G.B. Vertical Stripe
Display Mode		Normally White
White Luminance (ILED= 300mA) (Note: ILED is LED current)	[cd/m2]	275 typ.
Contrast Ratio		500:1 typ.
Response Time	[ms]	12 typ.
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Power Consumption	[Watt]	9.2 typ. (Include Logic and BLU power)
Weight	[Grams]	560 typ.
Physical Size (Include bracket)	[mm]	282.2 X 168 X 11.6 typ.
Electrical Interface		1 channel LVDS
Surface Treatment		Anti-Glare
Support Color		262K/16.2M colors (RGB 6-bit/6-bit+FRC)
Temperature Range Operating Storage (Non-Operating)	 [oC] [oC]	 0 to +70 -20 to +70
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance ILED= 300mA				220	275	---	cd/m^2	1, 3, 5.
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)	50 50	60 60	--- ---	degree	3, 6
		ψ_H ψ_L	Vertical (Upper) CR = 10 (Lower)	30 45	35 55	--- ---		
Luminance Uniformity		δ_{5P}	5 Points	---	---	1.25		1, 2, 3
Contrast Ratio		CR		350	450	---		3, 4
Response Time		T_r	Rising	---	4	8	msec	3, 5
		T_f	Falling	---	8	16		
		T_{RT}	Rising + Fallingg	---	12	24		
Color / Chromaticity Coodinates (tentativly)	White	Wx	CIE 1931	0.28	0.33	0.38		3
		Wy		0.27	0.32	0.37		
	Red	Rx		0.60	0.65	0.70		
		Ry		0.29	0.34	0.39		
	Green	Gx		0.26	0.31	0.36		
		Gy		0.58	0.63	0.68		
	Blue	Bx		0.09	0.14	0.19		
		By		0.01	0.06	0.11		
NTSC		%		---	72	---		

Note 1: 5 points position (Ref: Active area)

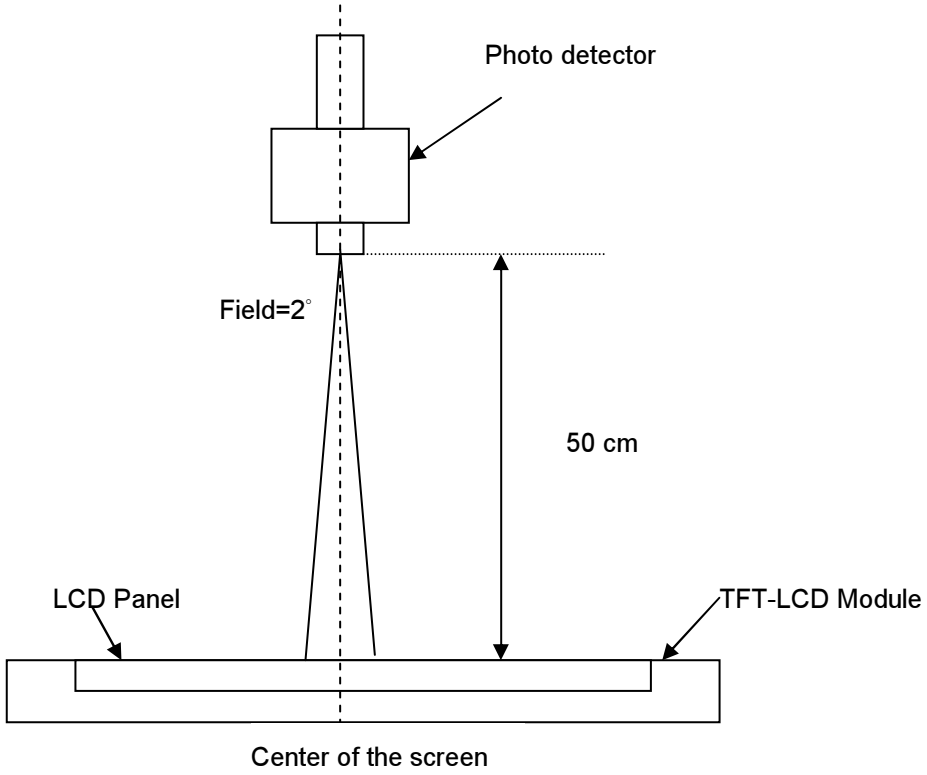


Note 2: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

Note 3: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



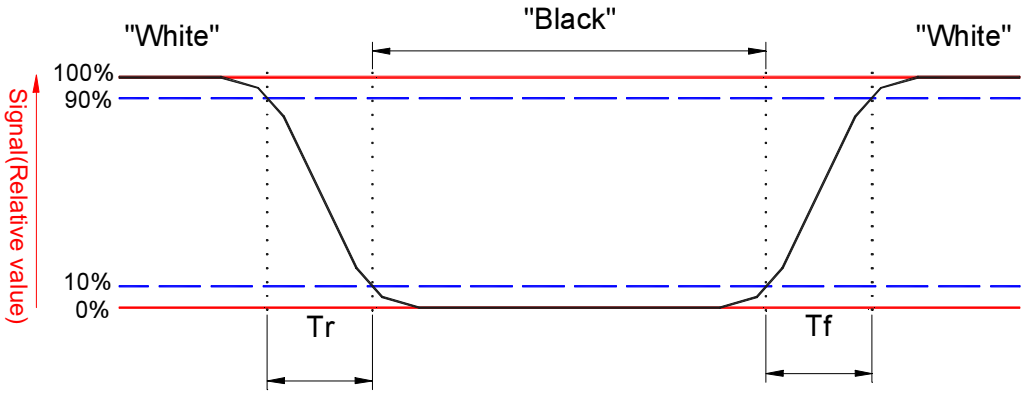
Note 4： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

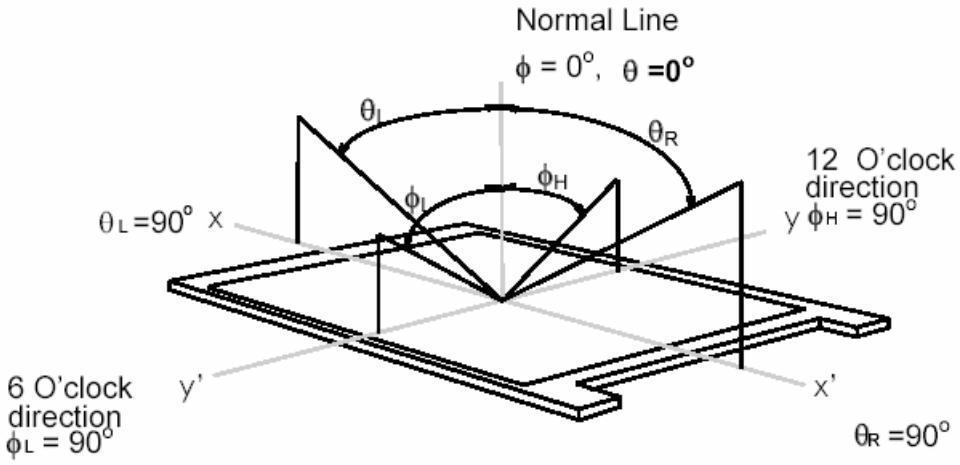
Note 5: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval is between 10% and 90% of amplitudes. Refer to figure as below.



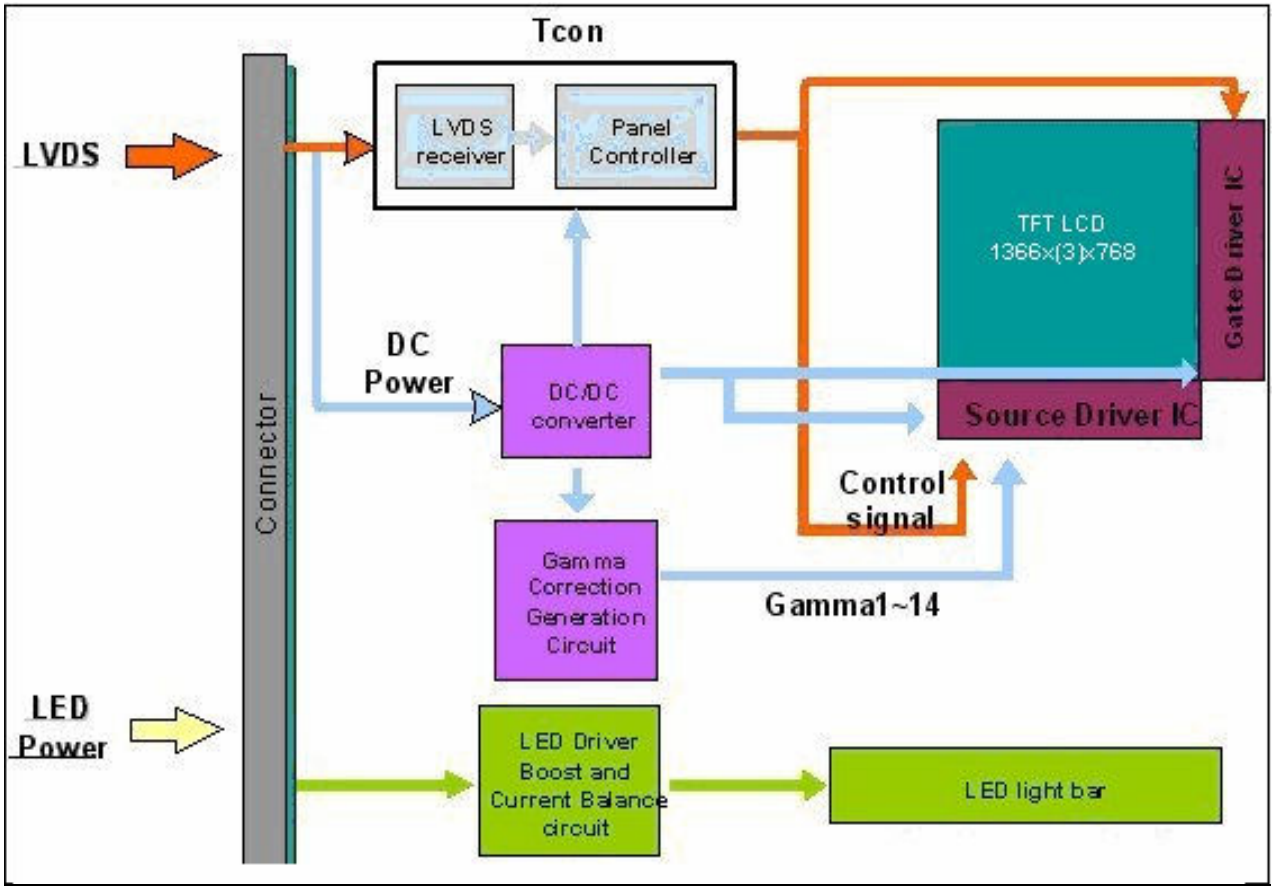
Note 6. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 11.6 inches wide Color TFT/LCD 30 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

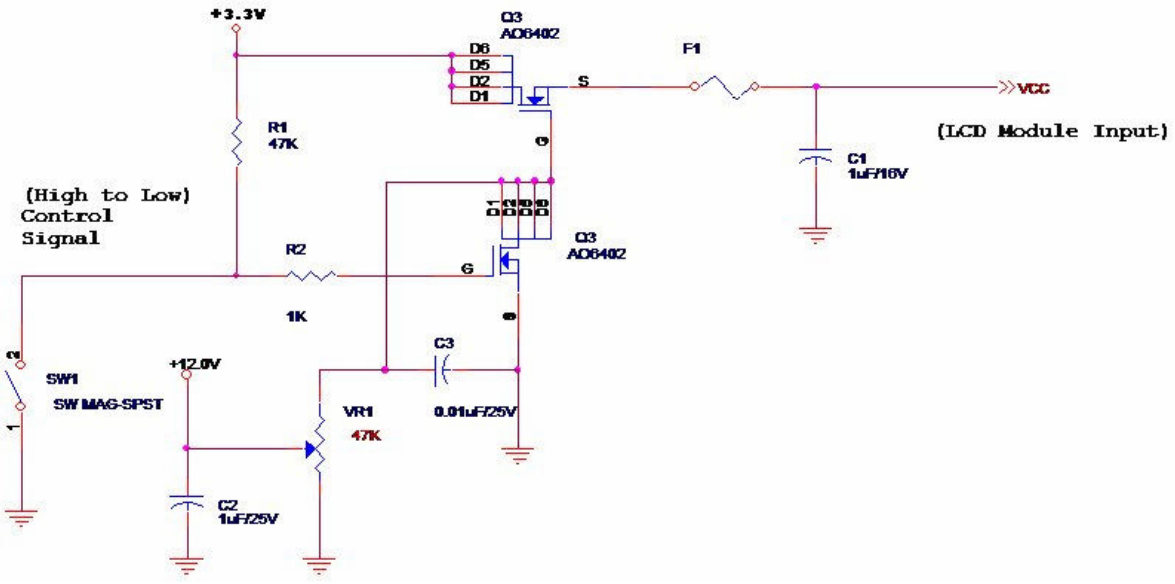
Input power specifications are as follows;

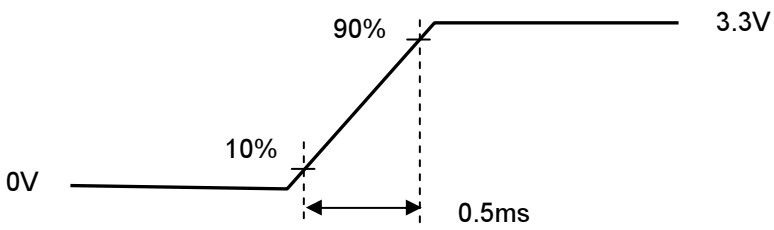
The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	---	0.8	0.9	[Watt]	Note 1
IDD	IDD Current	---	---	275	[mA]	Note 1
IRush	Inrush Current	---	---	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	---	---	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Black Pattern at 3.3V driving voltage. (P_{max}=$V_{3.3}$ x I_{black})

Note 2：Measure Condition





Vin rising time

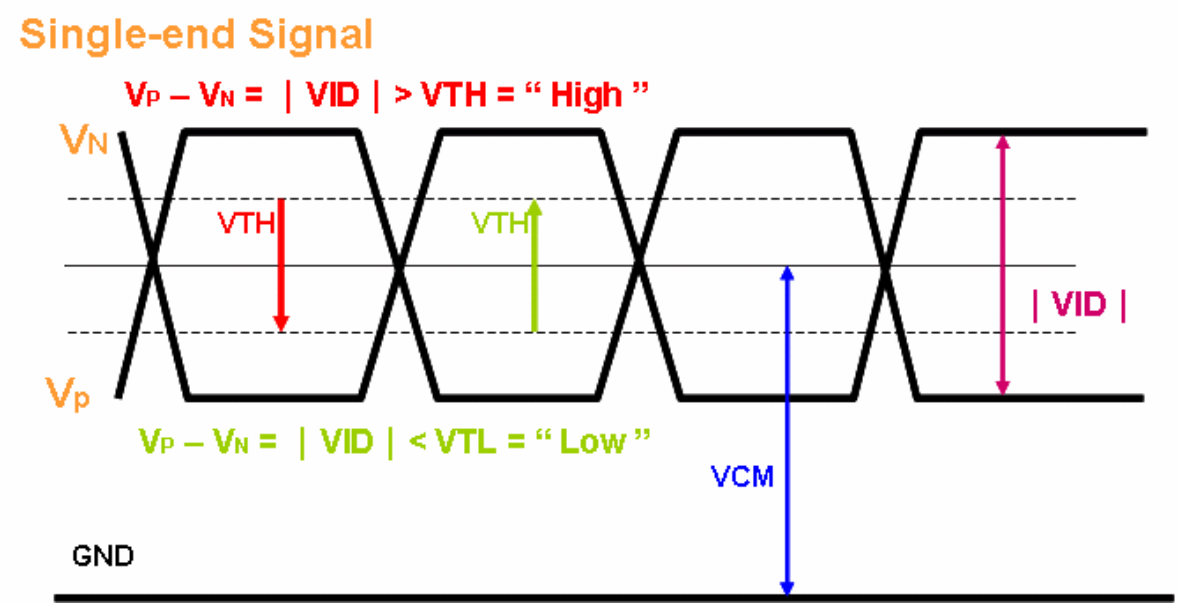
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{th}	Differential Input High Threshold (Vcm=+1.2V)	---	100	[mV]
V_{tl}	Differential Input Low Threshold (Vcm=+1.2V)	-100	---	[mV]
V_{ID}	Differential Input Voltage	100	600	[mV]
V_{cm}	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	---	8.4	11.5	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	30,000	---	---	Hour	(Ta=25℃), Note 2 I_F=300 mA

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

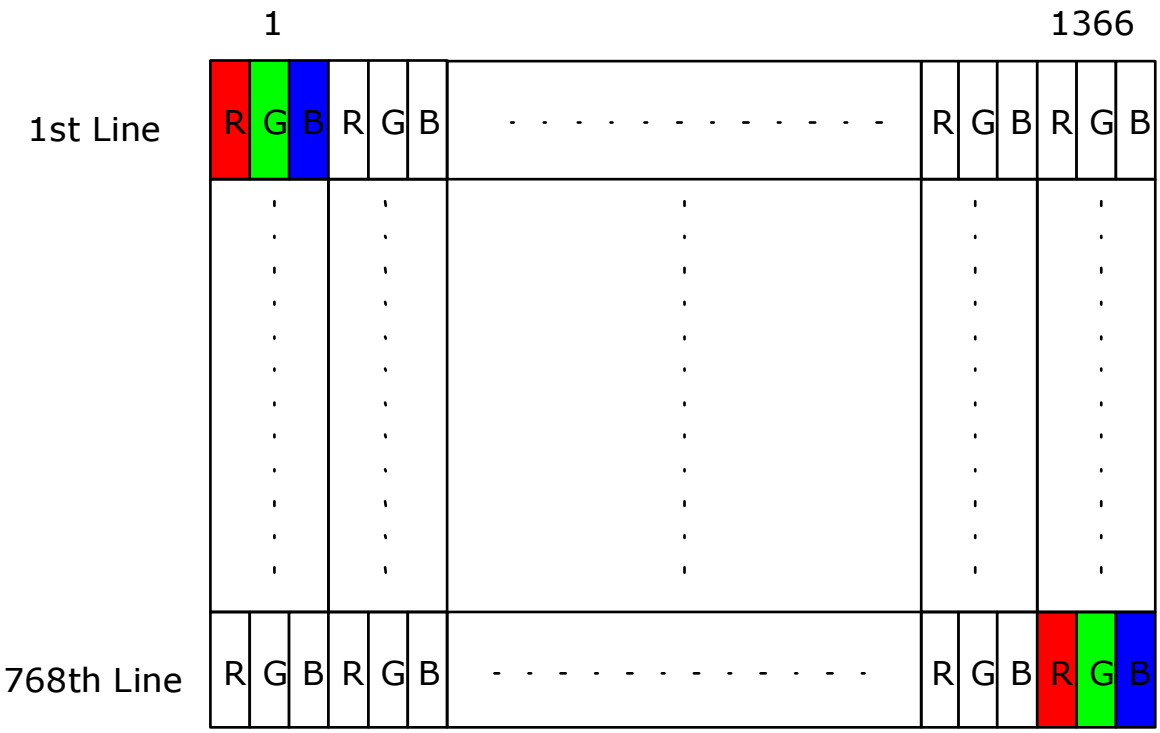
5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	10.8	12.0	13.5	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	3.0	3.3	3.6	[Volt]	
LED Enable Input Low Level		---	---	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	3.0	3.3	3.6	[Volt]	
PWM Logic Input Low Level		---	---	0.8	[Volt]	
PWM Input Frequency	FPWM	100		10K	Hz	
PWM Dimming Ratio	Duty	10	---	100	%	

6. Signal Interface Characteristic

6.1 Pixel Format Image

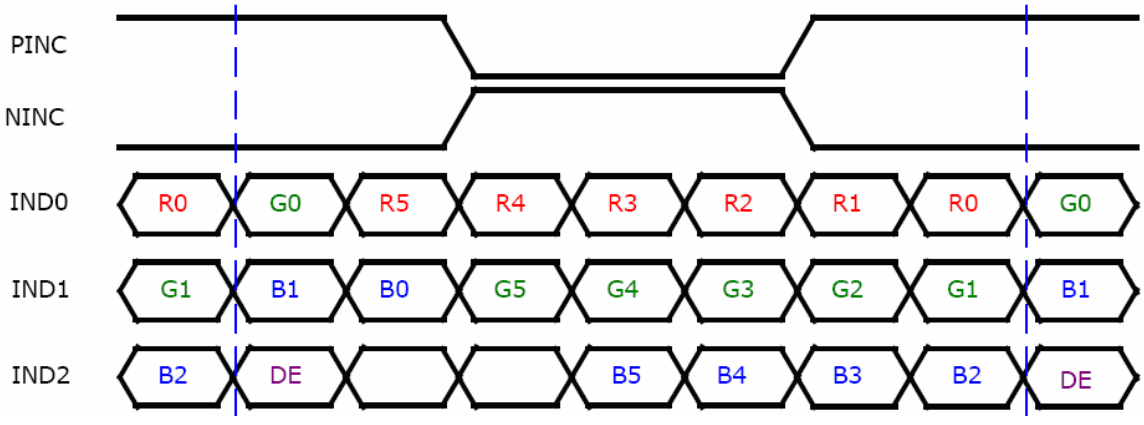
Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The Input Data Format (tentatively)

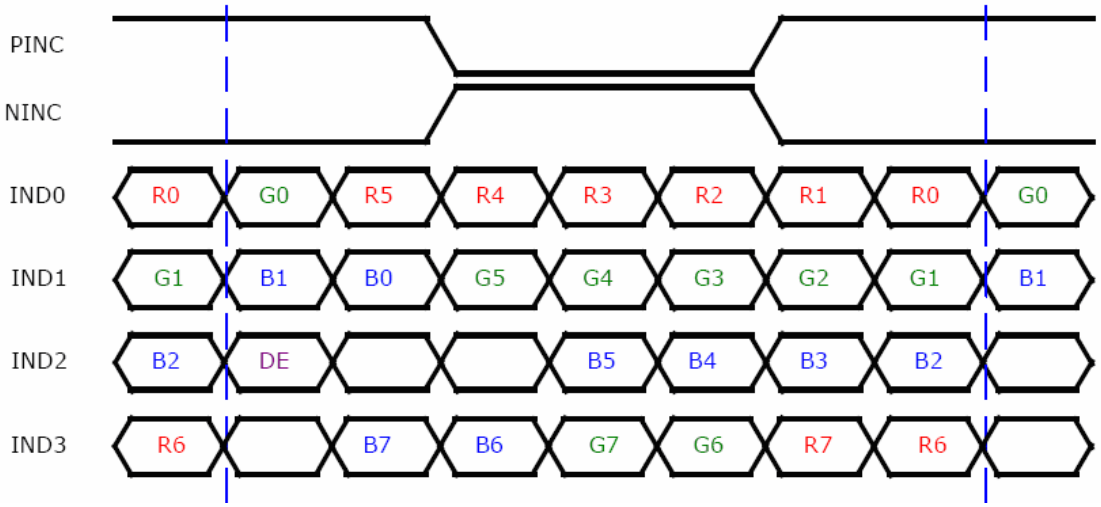
6/8 SEL = Low (GND)

6bits LVDS input➔When FRC='0', IND 3 pair fix to "Low"



6/8 SEL = High

8bits LVDS input→When FRC='1', IND 3 pair active



Signal Name	Description	
+RED5 +RED4 +RED3 +RED2 +RED1 +RED0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
+GREEN5 +GREEN4 +GREEN3 +GREEN2 +GREEN1 +GREEN0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE5 +BLUE4 +BLUE3 +BLUE2 +BLUE1 +BLUE0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
CLK	Data Clock	The typical frequency is 40MHz. The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of CLK. When the signal is high, the pixel data shall be valid to be displayed.

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

6.3 Integration Interface Requirement

6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	JAE or compatible
Connector Model Number	JAE FI-XPB30SL-HF10 (PCB Broken Type)
Mating Model Number	JAE FIX30HL or Compatible

6.3.2 Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

Pin No.	Symbol	Description
1	VDD	Power Supply, 3.3V (typical)
2	VDD	Power Supply, 3.3V (typical)
3	VSS	Ground
4	VSS	Ground
5	Rin0-	- LVDS differential data input
6	Rin0+	+ LVDS differential data input
7	VSS	Ground
8	Rin1-	- LVDS differential data input
9	Rin1+	+ LVDS differential data input
10	VSS	Ground
11	Rin2-	- LVDS differential data input
12	Rin2+	+ LVDS differential data input
13	VSS	Ground
14	ClkIN-	- LVDS differential clock input
15	ClkIN+	+ LVDS differential clock input
16	VSS	Ground
17	Rin3-	- LVDS differential data input (Used for 8 bit LVDS input)
18	Rin3+	+ LVDS differential data input (Used for 8 bit LVDS input)
19	VSS	Ground
20	VSS/SEL68	Select 6 or 8 Bits LVDS Input / Default Low (6Bits) Refer 1.6
21	VLED	Power Supply for LED 12V
22	VLED	Power Supply for LED 12V

23	VLED	Power Supply for LED 12V
24	GND	LED Ground
25	GND	LED Ground
26	GND	LED Ground
27	Dimming	Pulse width modulation (3.3V) for brightness of BLU control
28	Enable	LED BLU on/off control (on:3.3V, off: 0V)
29	GND	LED Ground
30	GND	LED Ground

Note: If 6-bit mode, please make sure that the voltage of Pin 18 is always lower than the voltage of Pin 17. (e.g. Pin 17: VDD, Pin 18: GND)

6.4 Interface Timing

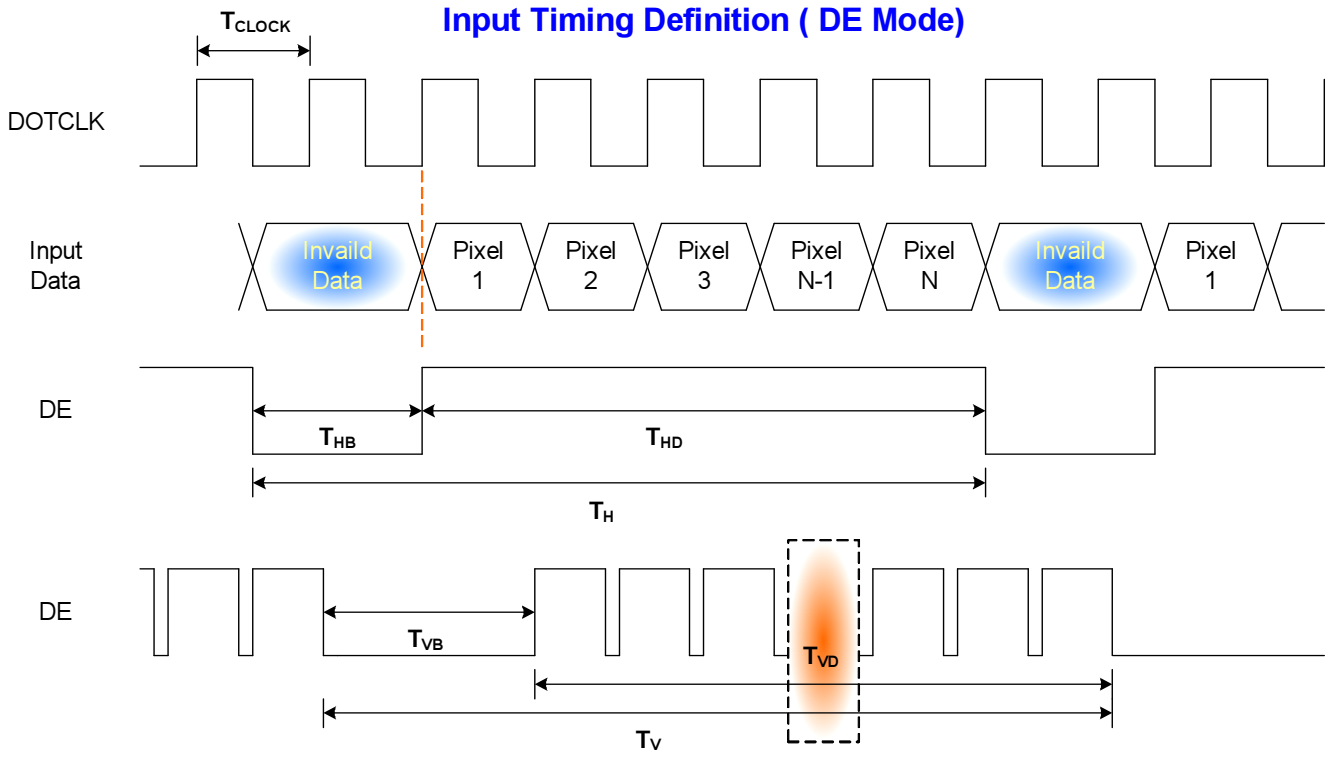
6.4.1 Timing Characteristics

Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		1/ T_{Clock}	65.5	70	80	MHz
Vertical Section	Period	T_V	776	808	1023	T_{Line}
	Active	T_{VD}	768			
	Blanking	T_{VB}	8	40	255	
Horizontal Section	Period	T_H	1406	1444	2047	T_{Clock}
	Active	T_{HD}	1366			
	Blanking	T_{HB}	40	78	681	

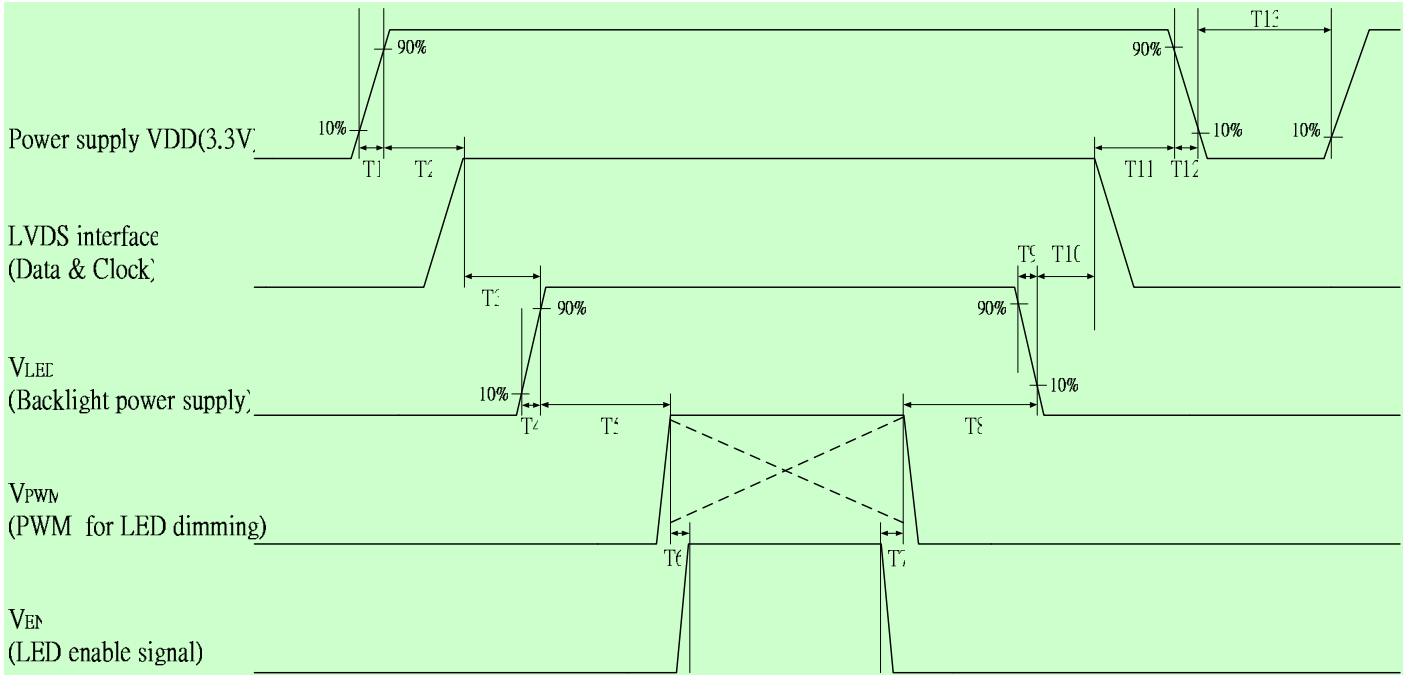
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



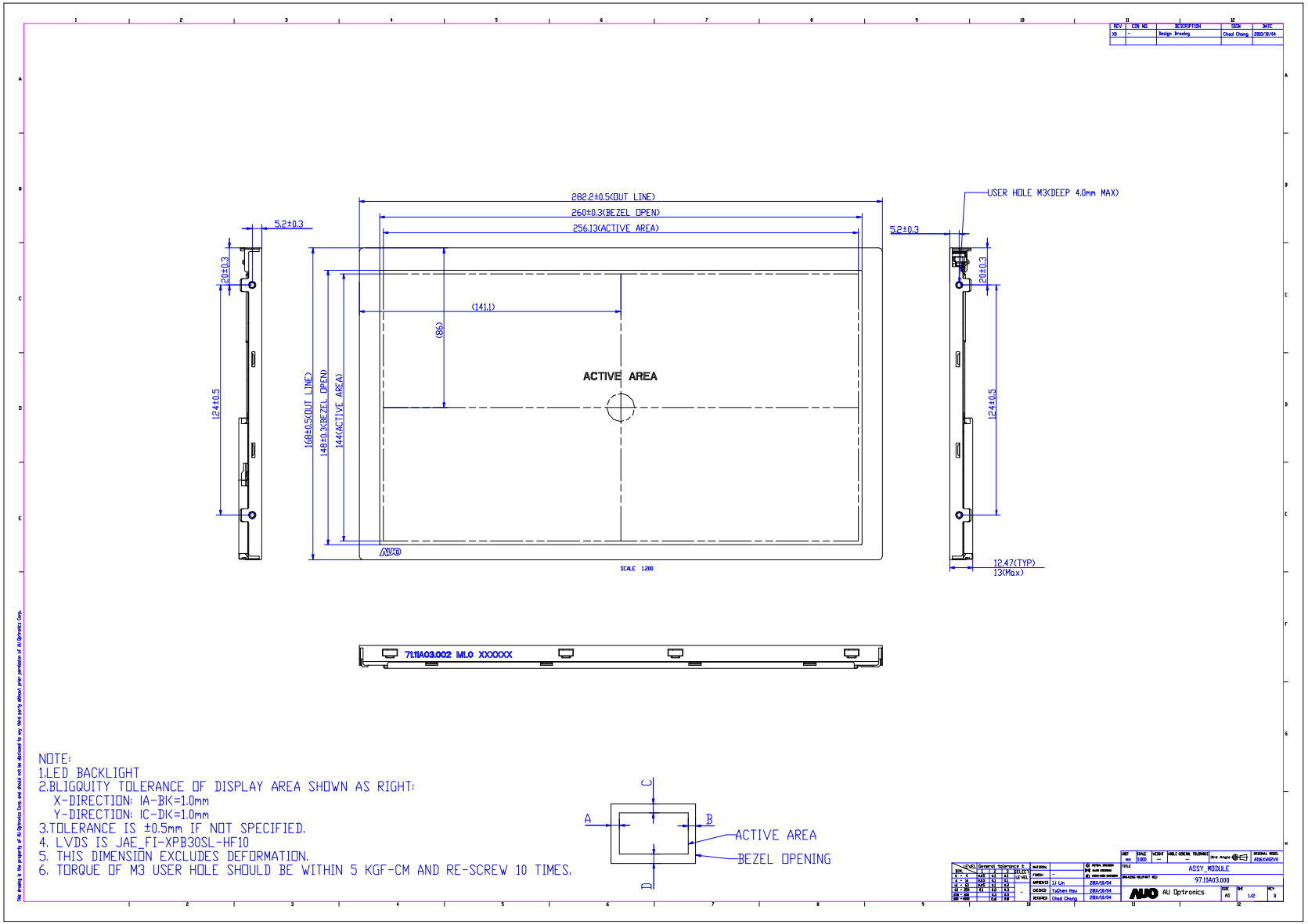
Power Sequence Timing				
Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	ms
T2	0	-	50	
T3	200	-	-	
T4	0.5	-	10	
T5	10	-	-	
T6	10	-	-	
T7	0	-	-	
T8	10	-	-	
T9	0	-	10	
T10	200	-	-	
T11	0.5	-	50	
T12	0	-	10	
T13	400	-	-	

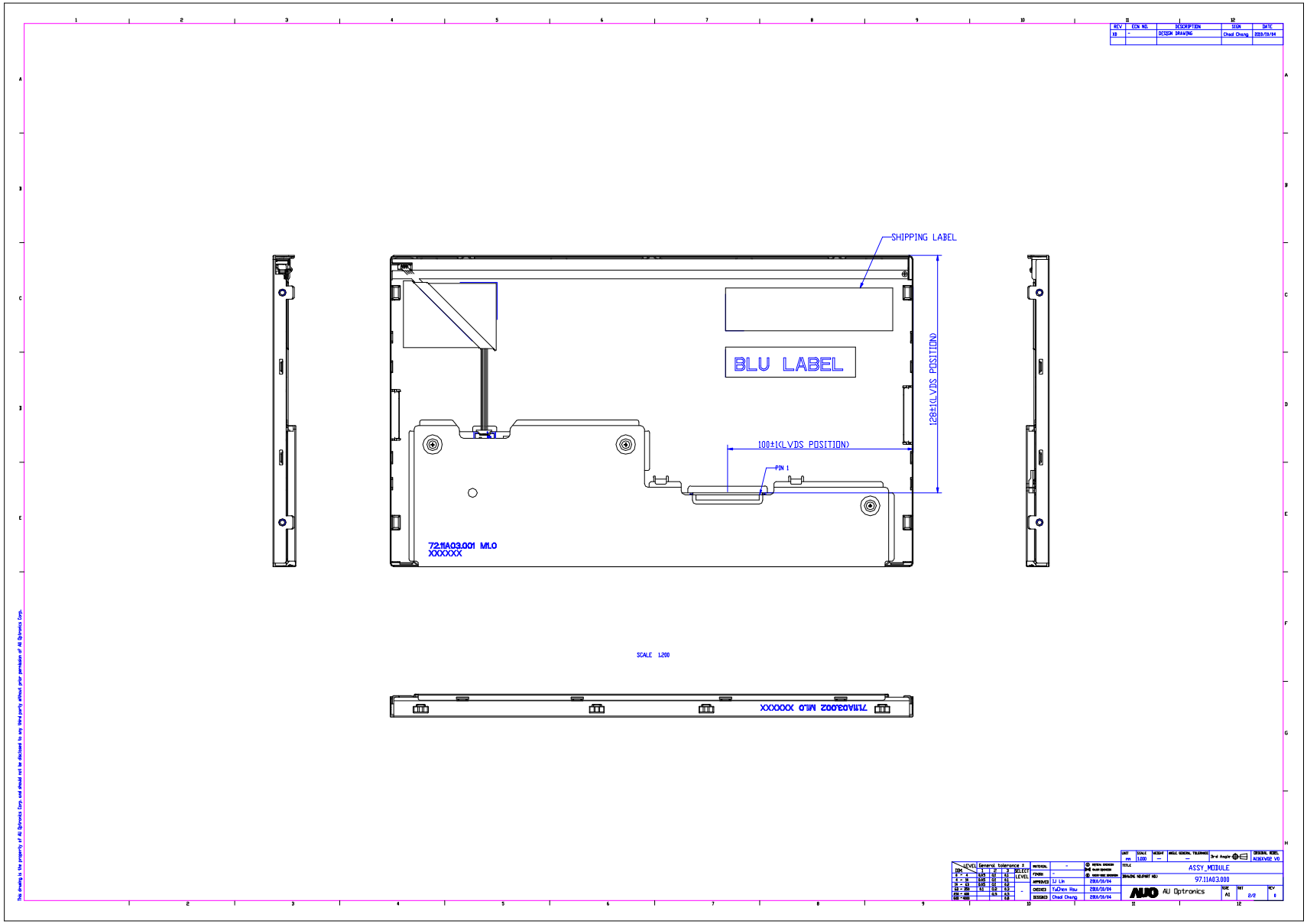
Note:If T3,T5,T6 couldn't match above specifications, must request T3+T5+T6 > 200ms at least

7. Panel Reliability Test

No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 70□ 240Hrs	
2	Low temperature storage	Ta= -20□ 240Hrs	
3	High temperature operation	Tp= 70□ 240Hrs	
4	Low temperature operation	Ta= 0□ 240Hrs	
5	High temperature and high humidity	Tp= 50□, 80% RH 240Hrs	Operation
6	Thermal shock	-20°C to +60°C, Ramp ≤20°C/min, Duration at Temp. = 30min, Test Cycles = 50	Non-operation
7	Vibration	Frequency range : 8~33.3Hz Stoke : 1.3mm Sweep : 3.0G, 33.3~400Hz Cycle : 15 minutes 2 hours for each direction of X,Z 4 hours for Y direction	JIS D1601, A-10 Condition A
8	Mechanical shock	100G, 6ms, ±X,±Y,±Z 3 times for each direction	JIS C0041, A-7 Condition C
9	Vibration (with carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/octave from 200~500Hz	IEC 68-34
10	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	JIS Z0202
11	Electro Static discharge (ESD)	Contact Discharge: ±8KV, 150pF(330Ω) 1sec, 8 points, 25 times point. Air Discharge: ± 15KV, 150pF(330Ω) 1sec, 8 points, 25 times/ point.	Operation & Non-operation

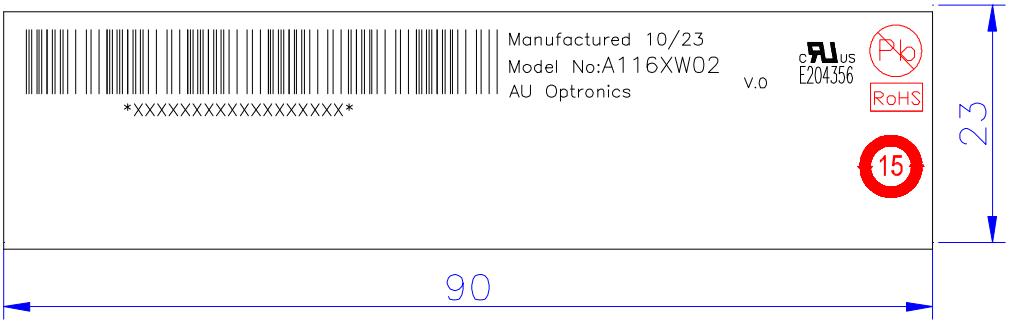
8. Mechanical Characteristics



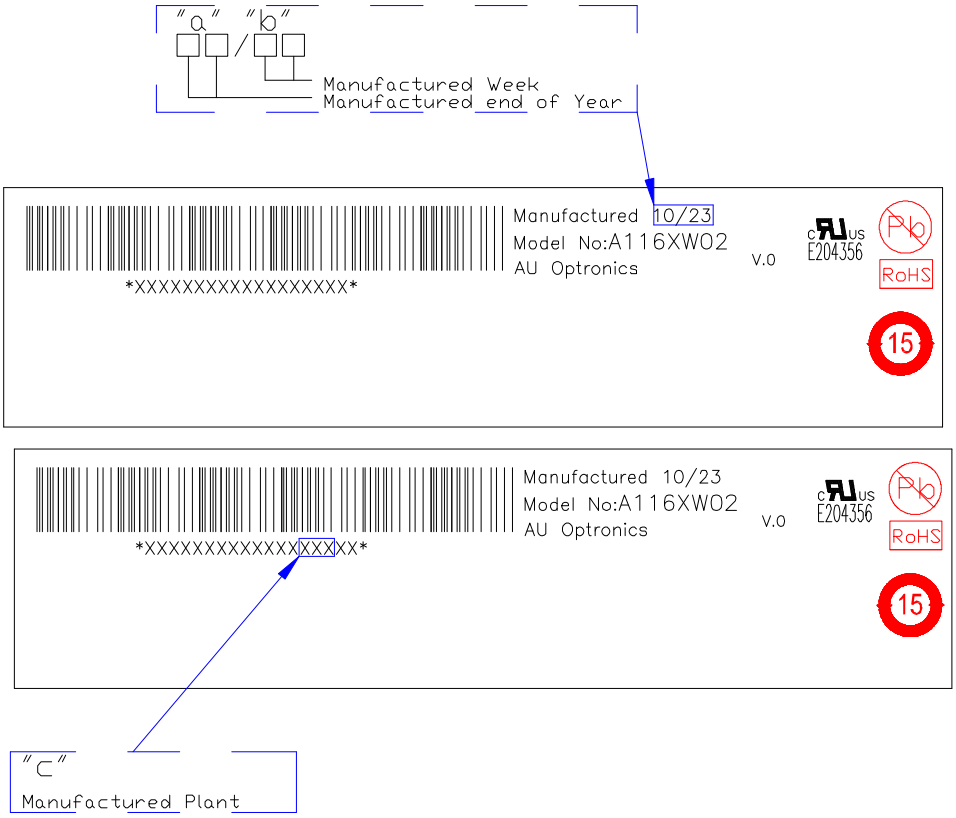

SHIPPING LABEL
BLU LABEL
128±1(LVDS POSITION)
100±1(LVDS POSITION)
PIN 1
SCALE 1:2.00
ASSY_MODULE
97.11A03.000
AU Optronics

9. Shipping and Packing

9.1 Shipping Label Format



9.2 Manufactured end of year and week mark



a. Manufactured end of year mark

Mark	05	06	07	08	…
Definition	2005	2006	2007	2008	…

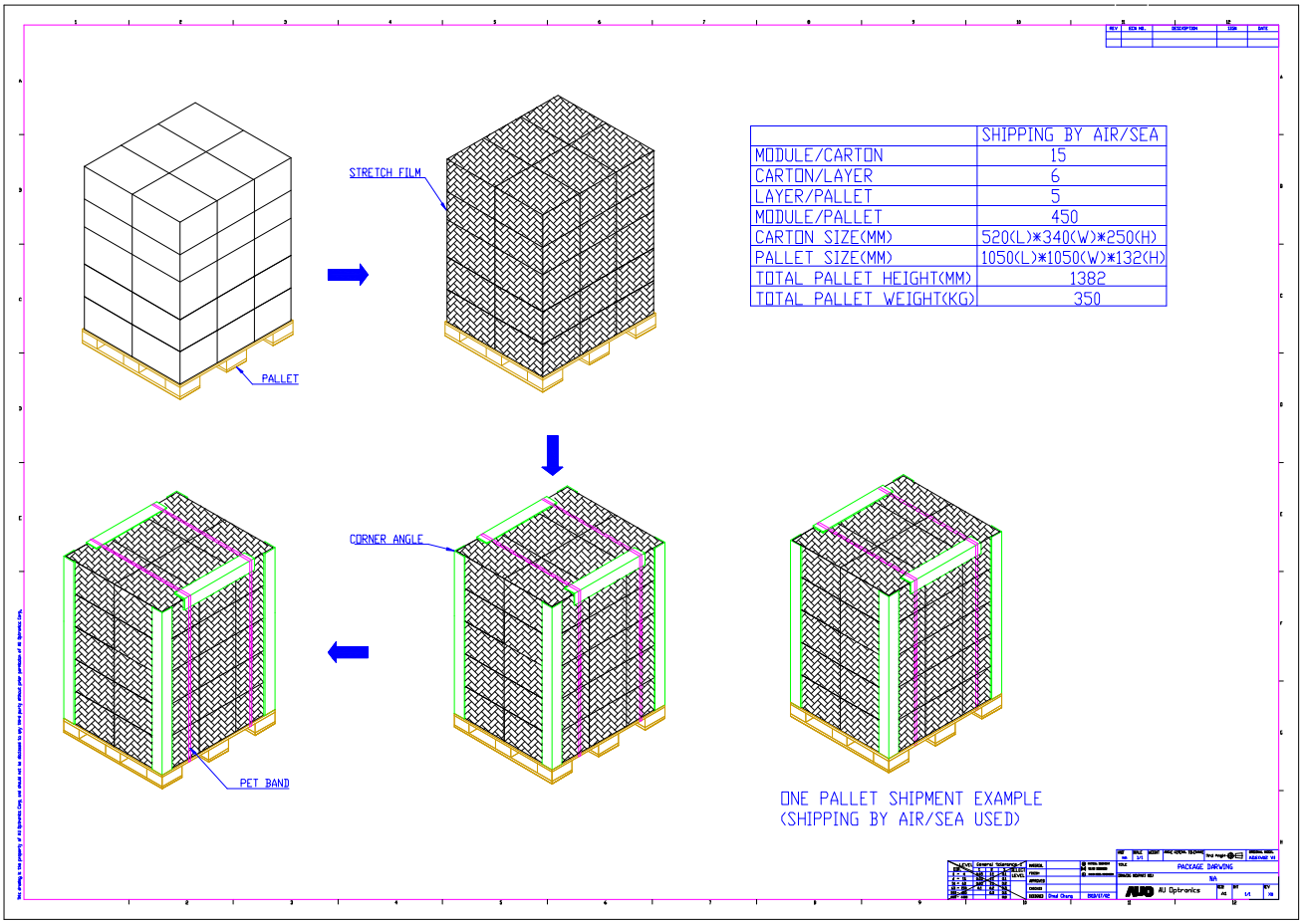
b. Manufactured week mark

Mark	01	02	…
Definition	1st Week	2nd Week	…

c. Manufactured Plant

Mark	M01	S01
Definition	Taiwan	China

9.3 Shipping Package of Palletizing Sequence



	SHIPPING BY AIR/SEA
MODULE/CARTON	15
CARTON/LAYER	6
LAYER/PALLET	5
MODULE/PALLET	450
CARTON SIZE(MM)	520(L)*340(W)*250(H)
PALLET SIZE(MM)	1050(L)*1050(W)*132(H)
TOTAL PALLET HEIGHT(MM)	1382
TOTAL PALLET WEIGHT(KG)	350